

AD - Converter

ICL7116

Single Chip AD – Converter for LCD

DATASHEET

OEM – Intersil

Source: Intersil Databook 1987

ICL7116/7117

ICL7116/7117**INTERSIL****ABSOLUTE MAXIMUM RATINGS****ICL7116**

Supply Voltage (V ⁺ to V ⁻)	15V
Analog Input Voltage (either input) (Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
HLDR, Clock Input	Test to V ⁺
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

ICL7117

Supply Voltage V ⁺	+6V
V ⁻	-9V
Analog Input Voltage (either input) (Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
HLDR, Clock Input	Gnd to V ⁺
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu\text{A}$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0.0V Full Scale = 200.0mV	-000.0	± 000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	V _{IN} \cong 200.0mV	-1	± 0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V (Note 7)	-1	± 0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V _{CM} = $\pm 1\text{V}$, V _{IN} = 0V, Full Scale = 200.0mV		50		$\mu\text{V}/\text{V}$
Noise (Pk — Pk value not exceeded 95% of time)	V _{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V _{IN} = 0V (Note 7)		1	10	pA
Zero Reading Drift	V _{IN} = 0 0°C < T _A < 70°C (Note 7)		0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV 0°C < T _A < 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V ⁺ Supply Current (Does not include LED current for 7117)	V _{IN} = 0		0.8	1.8	mA
V ⁻ Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25k Ω between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25k Ω between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		k Ω
V _{IL} , Pin 1 (7116 only)				TEST + 1.5	V

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NOTE: All typical values have been characterized but are not tested.

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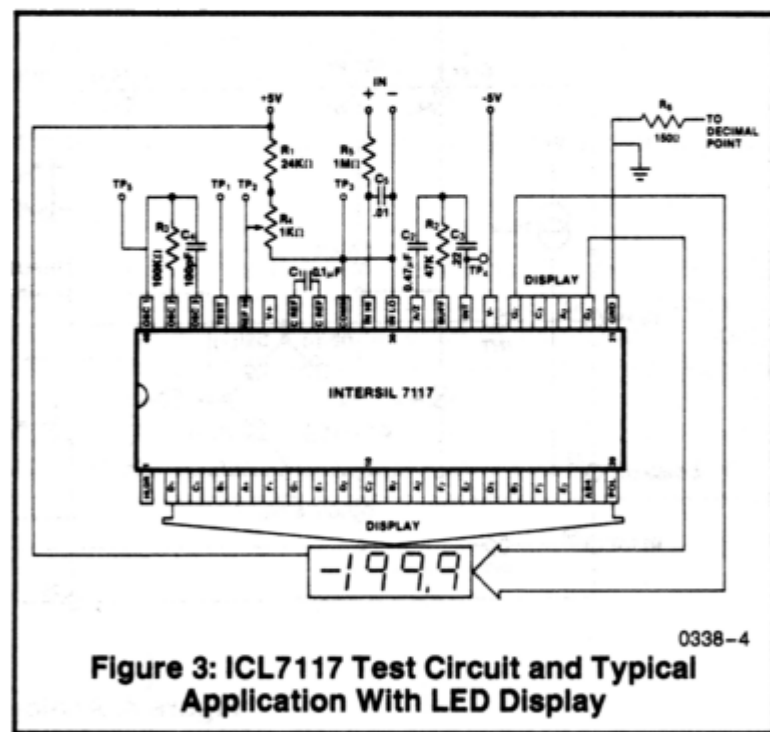
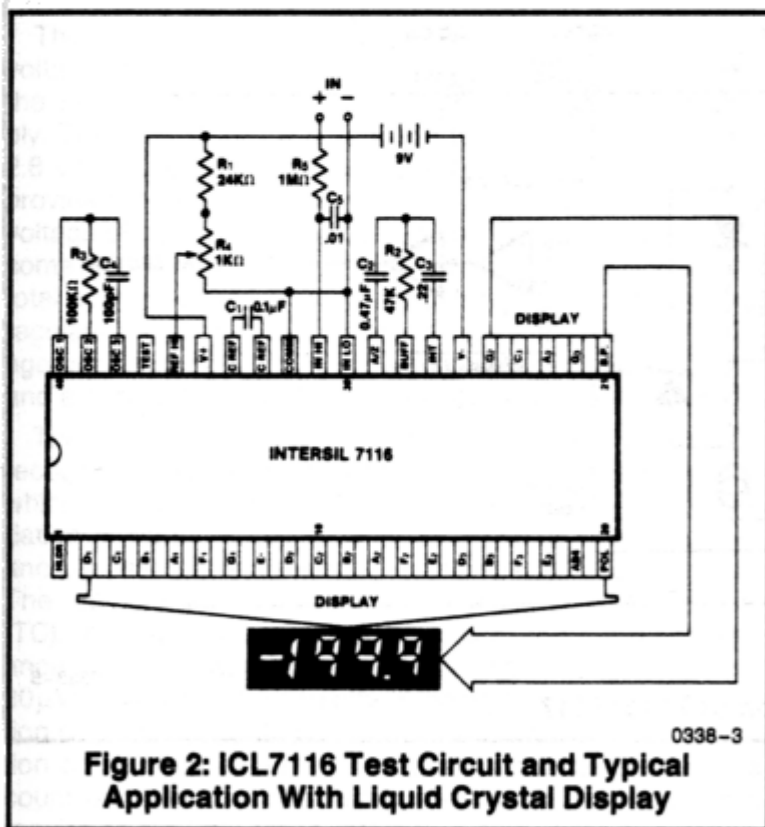
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ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL} , Pin 1 (7117 only)				GND + 1.5	V
V_{IH} , Pin 1 (Both)		$V^+ - 1.5$			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19 and 20) (Pin 19 only) (Pin 20 only)	$V^+ = 5.0V$ Segment Voltage = 3V	5 10 4	8.0 16 7		mA

- NOTES:**
- Unless otherwise noted, specifications apply to both the 7116 and 7117 at $T_A = 25^\circ C$, $f_{clock} = 48kHz$. 7116 is tested in the circuit of Figure 2. 7117 is tested in the circuit of Figure 3.
 - Refer to "Differential Input" discussion.
 - Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
 - The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.
 - Not tested, guaranteed by design.

TEST CIRCUITS



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DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and

low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$1000 \left(\frac{V_{in}}{V_{ref}} \right)$$

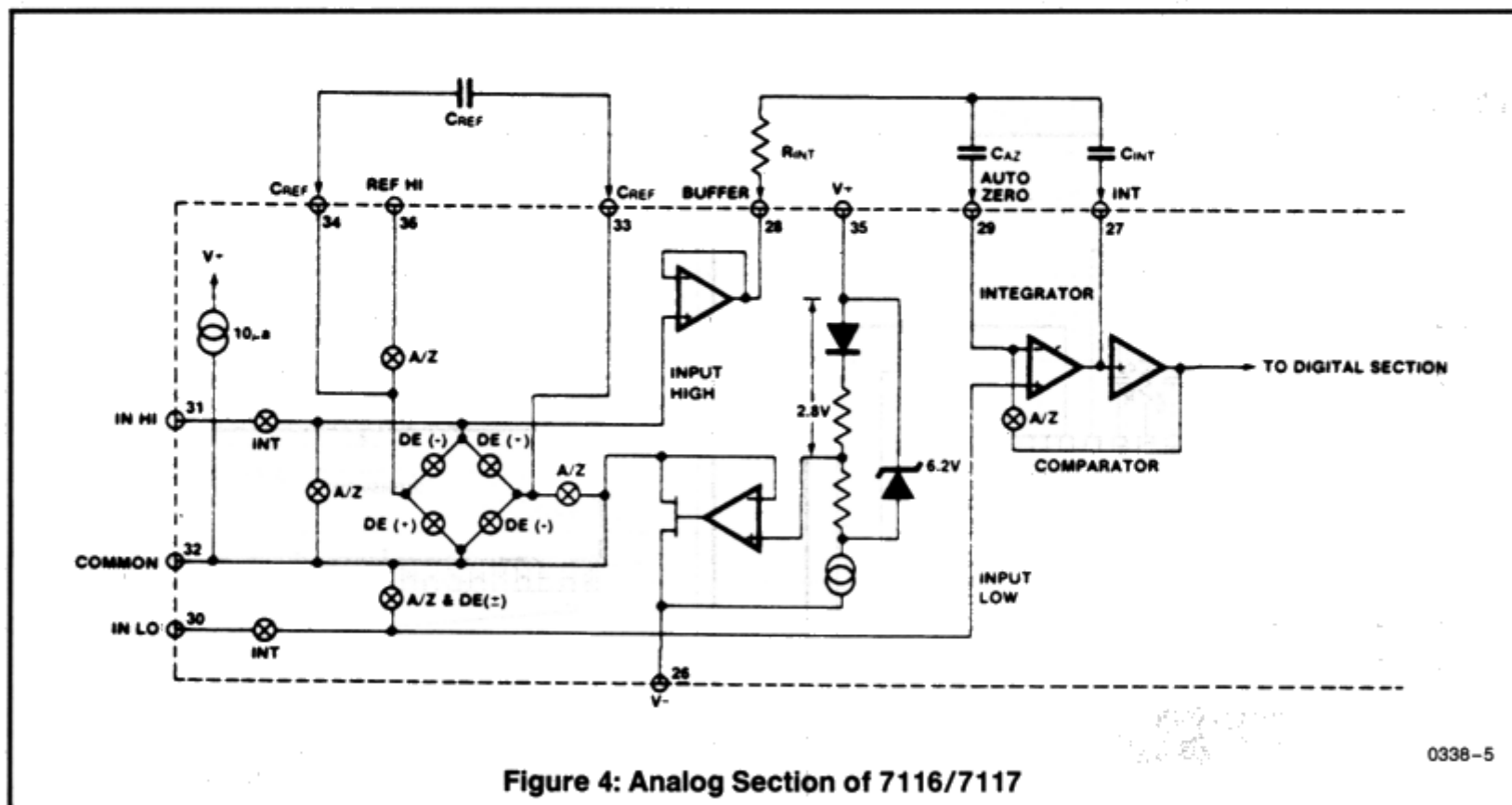


Figure 4: Analog Section of 7116/7117

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Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of typically 86dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See Application Note A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts less than the positive supply. This is selected to provide proper operation with a minimum end-of-life battery voltage of about 6V. However, analog COMMON does have some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($> 7V$), the COMMON voltage will have a low voltage coefficient ($.001\%/V$), low output impedance ($\approx 15\Omega$), and a temperature coefficient typically less than $80\text{ppm}/^\circ\text{C}$.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from $25\mu\text{V}$ to $80\mu\text{Vpk-pk}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

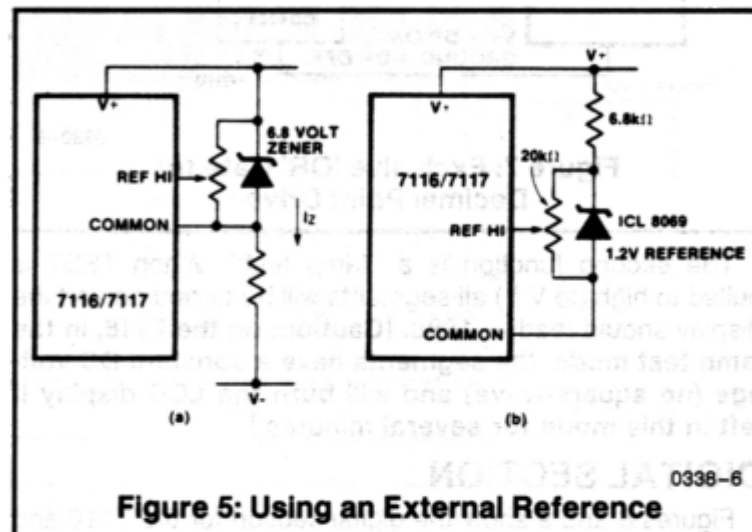


Figure 5: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only $10\mu\text{A}$ of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.

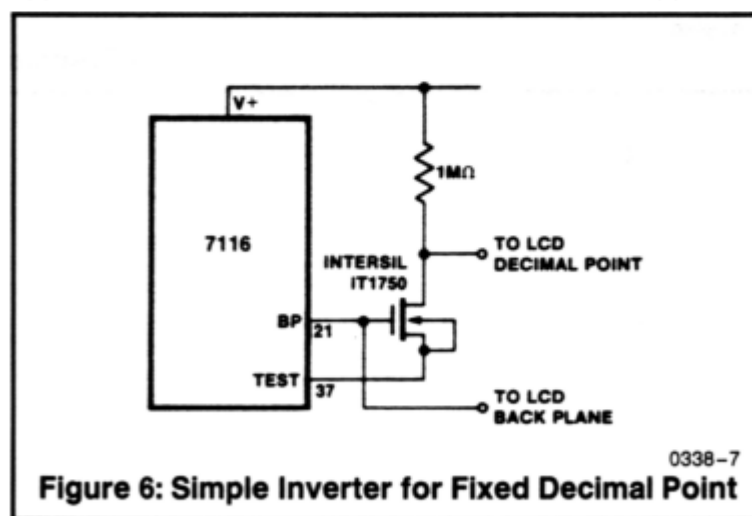


Figure 6: Simple Inverter for Fixed Decimal Point

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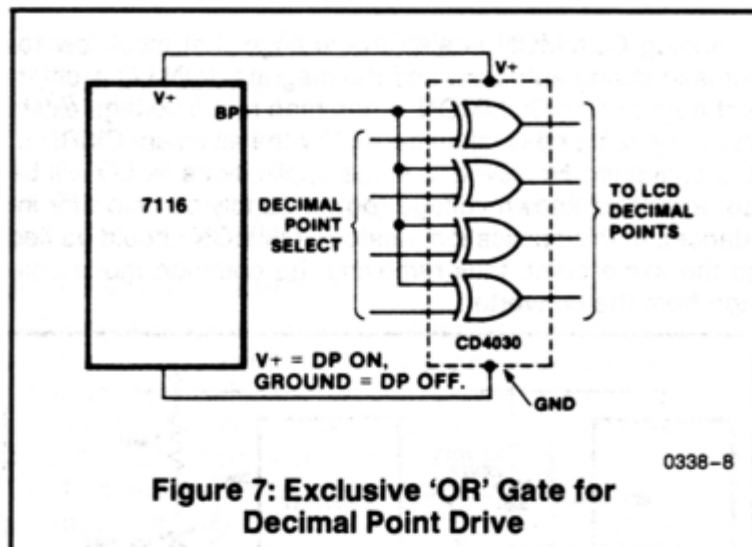


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read - 1888. [Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7117. It is identical to that of the 7116 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70k Ω typical resistance to either TEST (7116) or GROUND (7117).

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DISPLAY FONT

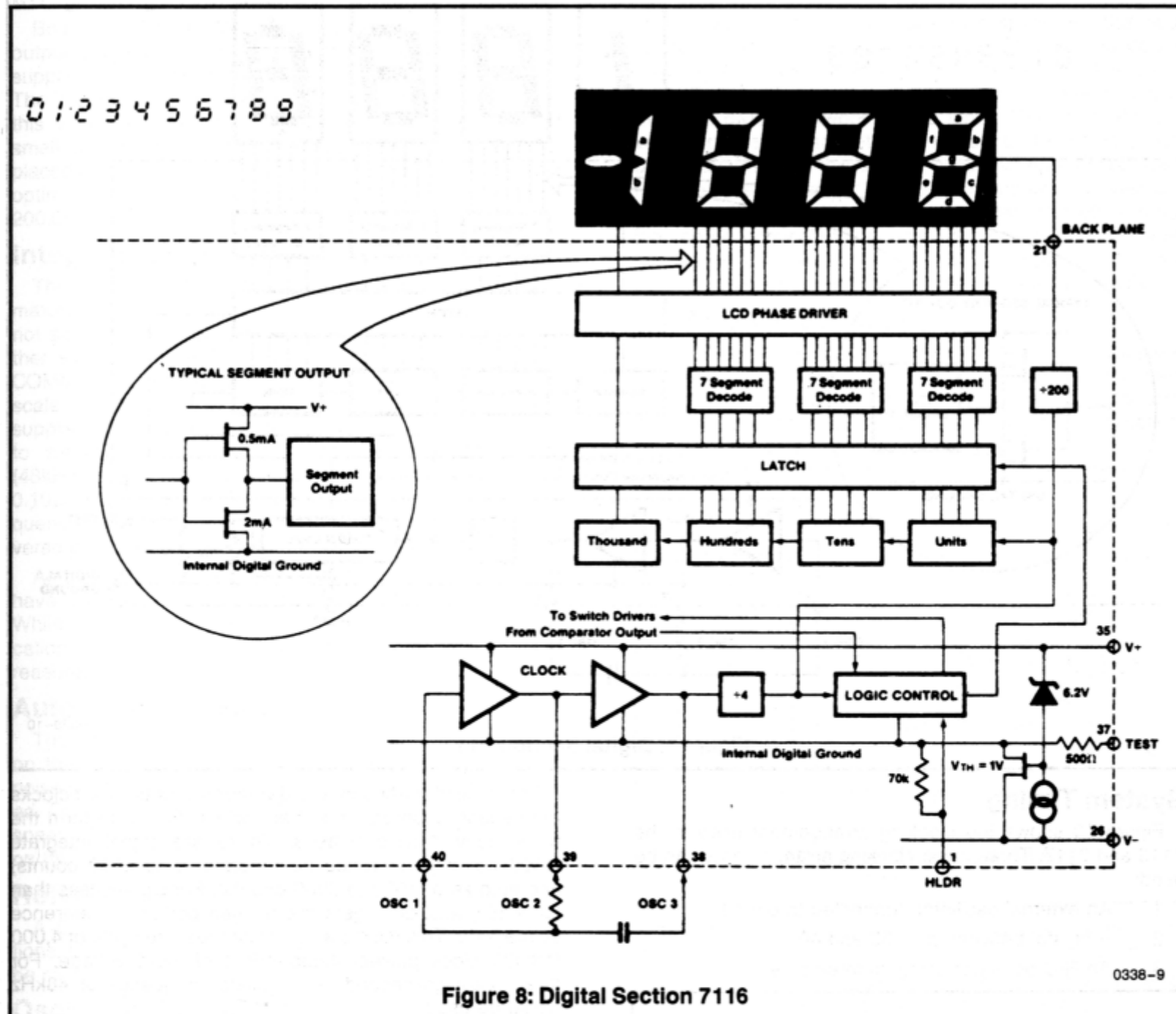


Figure 8: Digital Section 7116

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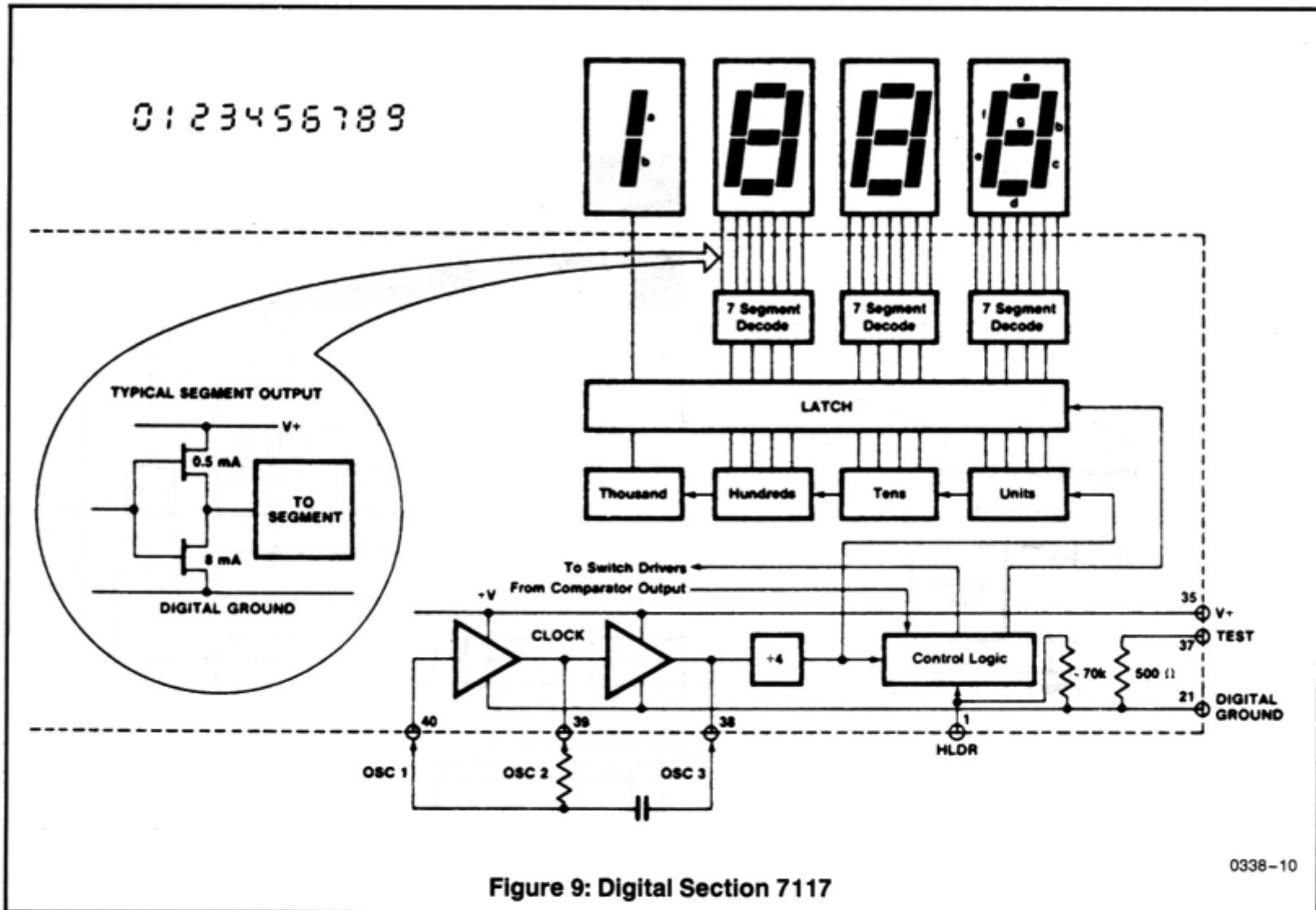


Figure 9: Digital Section 7117

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System Timing

Figure 10 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

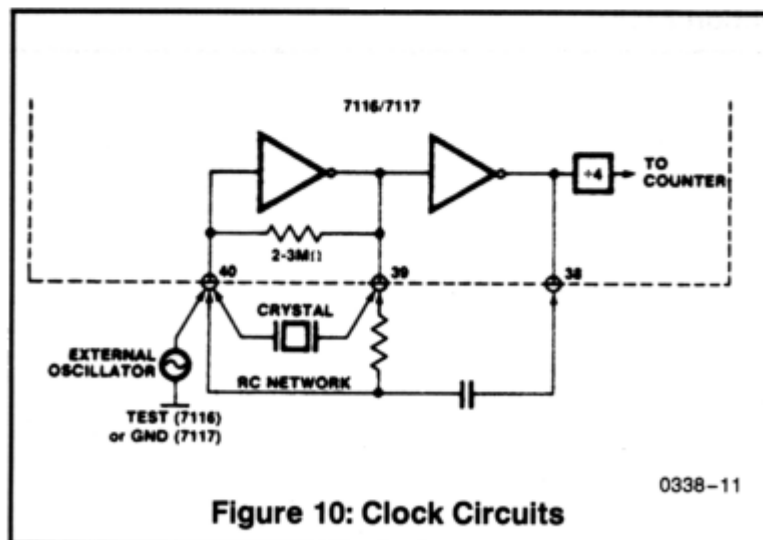


Figure 10: Clock Circuits

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COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with $100\mu\text{A}$ of quiescent current. They can supply $20\mu\text{A}$ of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volts full scale, $470\text{k}\Omega$ is near optimum and similarly a $47\text{k}\Omega$ resistor is optimum for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ± 2 volt full scale integrator swing is fine. For the 7117 with ± 5 volt supplies and analog common tied to supply ground, a ± 3.5 to ± 4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are $0.22\mu\text{F}$ and $0.10\mu\text{F}$, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a $0.47\mu\text{F}$ capacitor is recommended. On the 2 volt scale, a $0.047\mu\text{F}$ capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A $0.1\mu\text{F}$ capacitor gives good results in most applications. If rollover errors occur a larger value, up to $1.0\mu\text{F}$ may be required.

Oscillator Components

For all ranges of frequency a $100\text{k}\Omega$ resistor is recommended and the capacitor is selected from the equation $f \approx \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), $C = 100\text{pF}$.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{\text{IN}} = 2V_{\text{REF}}$. Thus, for the 200.0mV and 2.000 volt scale, V_{REF} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the

digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V . Instead of dividing the input down to 200.0mV , the designer should use the input voltage directly and select $V_{\text{REF}} = 0.341\text{V}$. Suitable values for integrating resistor and capacitor would be $120\text{k}\Omega$ and $0.22\mu\text{F}$. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ± 5 volts supplies can accept input signals up to ± 4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{\text{IN}} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7117 Power Supplies

The 7117 is designed to work from ± 5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

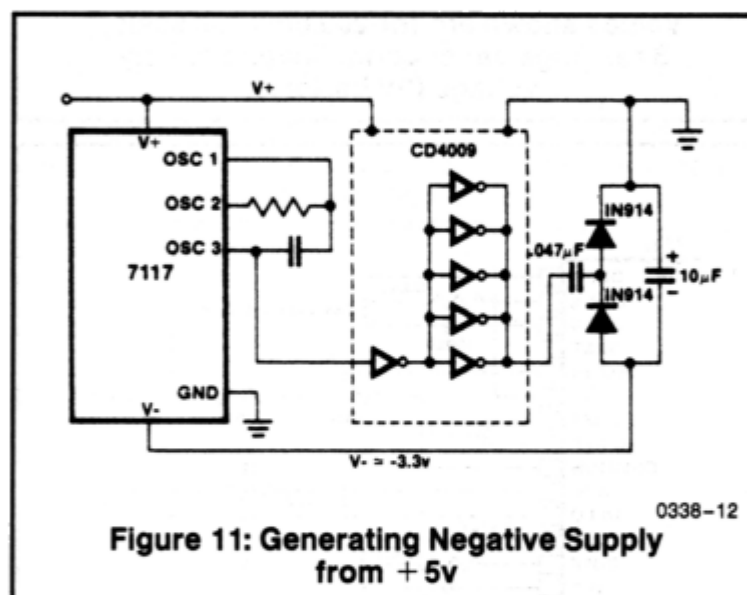


Figure 11: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ± 1.5 volts in magnitude.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

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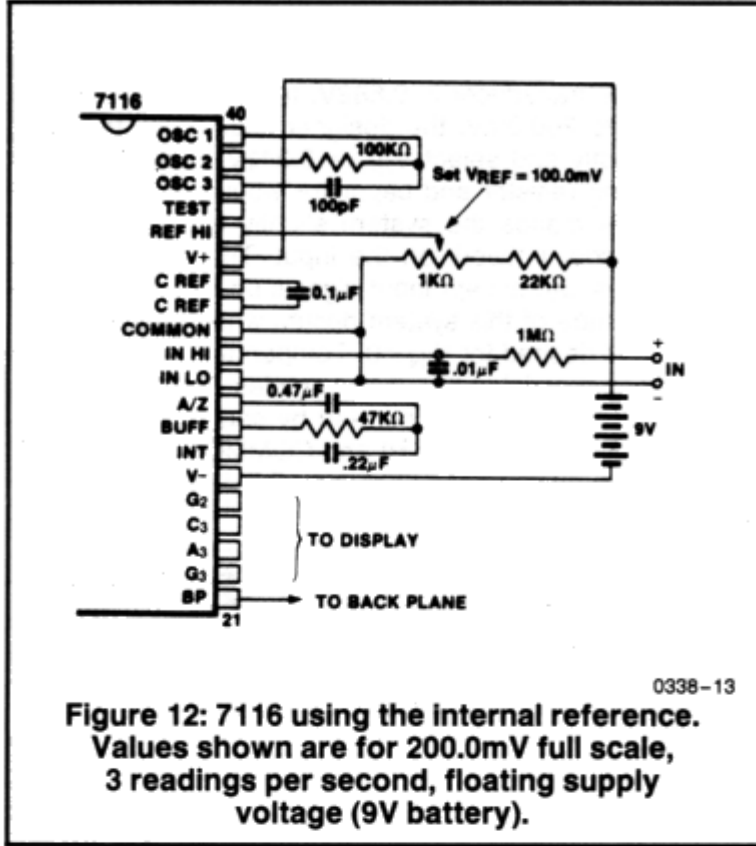


Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

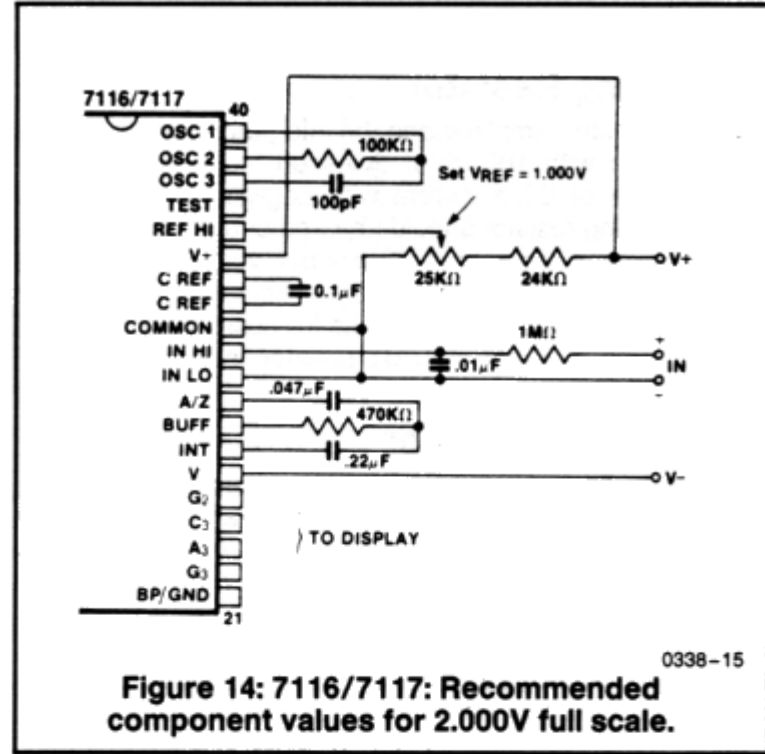


Figure 14: 7116/7117: Recommended component values for 2.000V full scale.

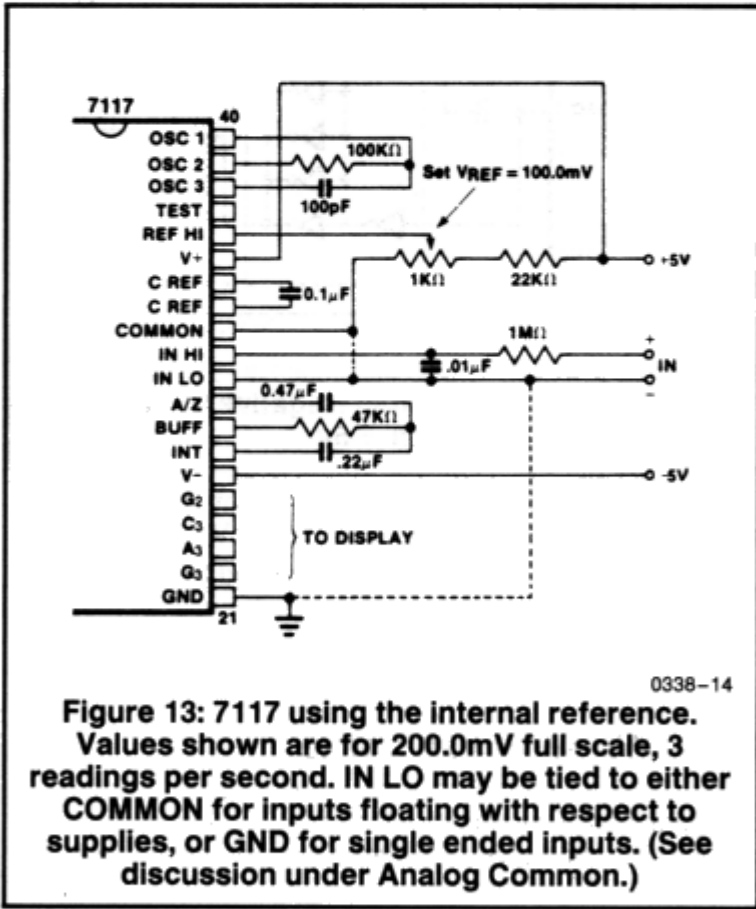


Figure 13: 7117 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)

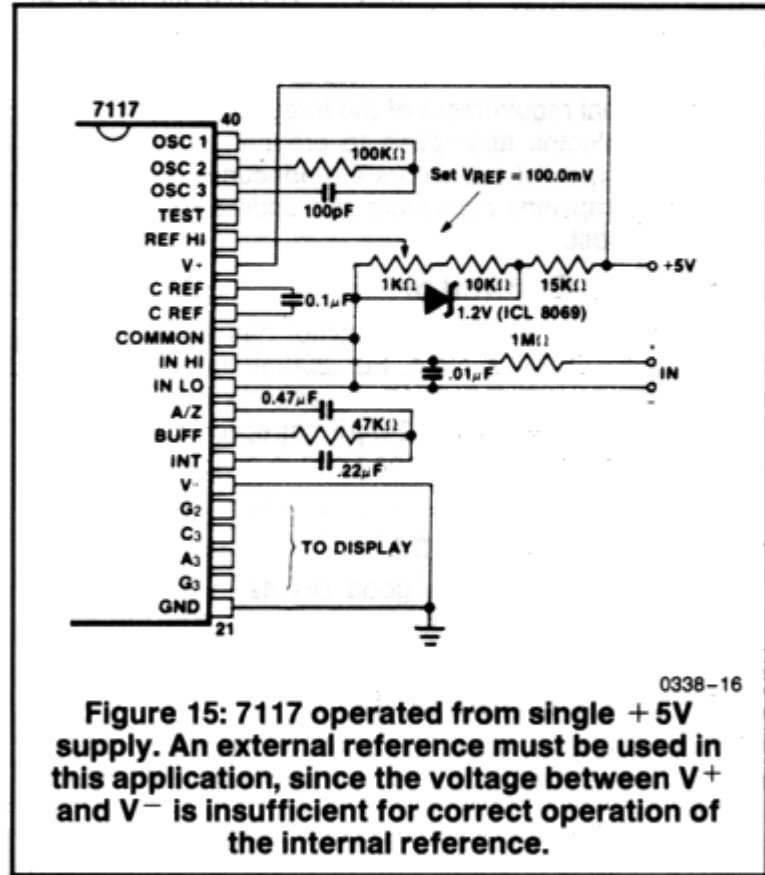


Figure 15: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

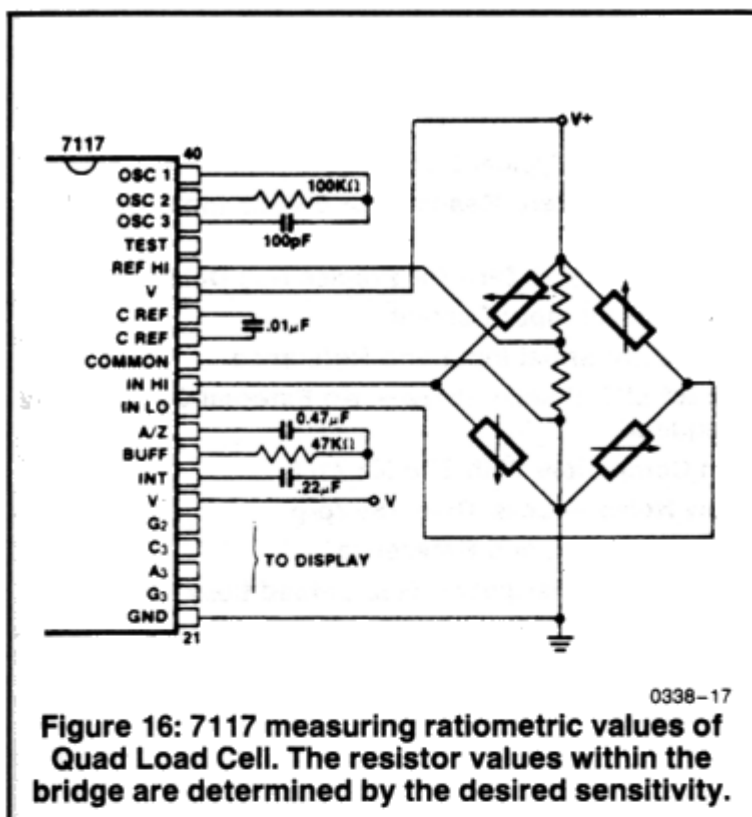
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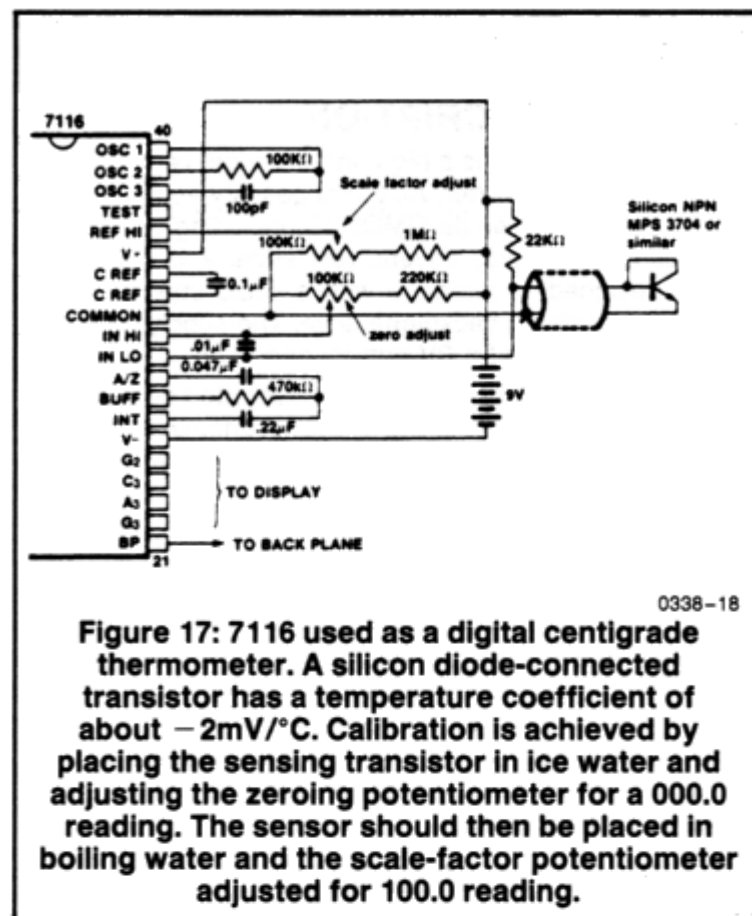
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0338-17
Figure 16: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.



0338-18
Figure 17: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

- A016** "Selecting A/D Converters," by David Fullagar.
- A017** "The Integrating A/D Converter," by Lee Evans.
- A018** "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A023** "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032** "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046** "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047** "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
- A052** "Tips for Using Single-Chip $3\frac{1}{2}$ -Digit A/D Converters," by Dan Watson.

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